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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/903,521	07/13/2001	Satoshi Nakamura	325772024100	2646

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EXAMINER

TRAN, NHAN T

ART UNIT PAPER NUMBER

2615

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/903,521

Applicant(s)

NAKAMURA, SATOSHI

Examiner

Nhan T. Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4,6 and 18-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4,6 and 18-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-2, 4, 6, 18-20 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al (US 2003/0164884 A1) in view of Wong et al (US 2003/0058355 A1).

Regarding claim 1, Morris discloses a solid-state image sensing apparatus (Fig. 13), comprising:

a solid-state image sensing device (119, Fig. 3) outputting an electrical signal proportional to an intensity of incident light, the solid-state image sensing device configured for outputting a first signal converted linearly to the intensity of the incident light and a second

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signal converted natural-logarithmically to the intensity of the incident light (see paragraph [0022]);

a first signal processing circuit (i.e., a first portion of pre-processing circuit 126) supplied with the first signal from the solid-state sensing device and performing double correlated sampling processing (paragraph [0034]);

a second signal processing circuit (i.e., a second portion of pre-processing circuit 126) supplied with the second signal from the solid-state image sensing device and performing double correlated sampling processing (paragraph [0034]).

Morris does not explicitly teach a plurality of color filters provided in the solid-state image sensing device, wherein the first signal and the second signal output from the solid-state image sensing apparatus comprise a plurality of color signals. Morris neither teaches that the first and second signal processing circuits perform white balancing adjustment of the first signal and the second signal, respectively, and wherein a dynamic range of the second signal is adjusted at the second signal processing circuit thereby a contrast of the second signal is improved.

As taught by Wong in Fig. 1 and paragraph [0034], a pre-processing circuit 115 not only performs correlated double sampling and color filter array interpolation (implying that an image sensor has a plurality of color filters provided thereon) but the pre-processing circuit 115 also performs white balancing and gain control for optimizing dynamic range of the image signals.

Therefore, it would have been obvious to one of ordinary skill in the art to provide a plurality of color filters on the image sensor device (119) in a conventional way so as to output the first and second signals in color signals, and further to expand the first and second pre-processing circuits in Morris by incorporating white balancing processing, gain control

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processing in addition to the correlated double sampling so that the dynamic range/contrast of the output signals are enhanced.

Regarding claim 18, see the analysis of claim 1.

Regarding claim 19, Morris clearly discloses in paragraph [0034] that signal processing circuit further comprising: a first signal processing circuit receiving the first signal from the solid-state image sensing device and performing *at least a portion* of the first predetermined signal processing; and a second signal processing circuit receiving the second signal from the solid-state image sensing device and performing *at least a portion* of the second predetermined signal processing.

Regarding claim 20, Morris further discloses the signal processing circuit comprising a third signal processing circuit (processing circuit 148) receiving the first and second signals processed by the first and second signal processing circuits (a first portion and a second portion of signal conditioning circuits 126 including noise filtering), respectively, and performing *at least a portion* of the first and second predetermined signal processing on the first and second signals (see Fig. 13; paragraph [0037] and note that the signal processing circuit 148 is coupled to the pre-processing circuit 126 to perform a part of *further* processing of the first and second signals).

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3. Claims 2, 4 & 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al. and Wong et al. as applied to claim 1 and in further view of D'Luna et al (US 5,008,739).

Regarding claim 2, the combination of Morris and Wong discloses the imaging sensing apparatus having all features as analyzed in claim 1. Morris further discloses a third signal processing circuit (148) to process signals output from the first and second signal processing circuits as analyzed in claim 20.

Morris and Wong fail to disclose a logarithmic/linear conversion circuit for converting a signal output from the second signal processing (in logarithmic mode) to a signal linearly proportional to the intensity of the incident light before inputting to the third signal processing circuit. D'Luna teaches a log to linear conversion circuit to convert the logarithmic signal to a linear signal for further processing at subsequent states (i.e., black level clamping) since the subsequent processes are desirably completed in linear space, where the adjustments will be direct, linear relation to the charge signal amplitudes existing on the image sensor (see col. 6, lines 1-11).

Therefore, it would have been obvious to one of ordinary skill in the art to include a log to linear conversion circuit on the output of the second signal processing circuit in Morris to convert the logarithmic signal to a linear signal before outputting the signal to the third signal processing for further processing such as black clamping which would require the signal in a linear space, where the adjustments would be direct, linear relation to the charge signal amplitudes existing on the image sensor.

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Regarding claim 4, both Wong and D'Luna further teach a gamma correction that would be included in the first processing circuit (for linear characteristics) and the second processing circuit (for logarithmic characteristics) for correcting gamma of the first signal and second signals, respectively. See Wong, paragraph [0-034] and D'Luna, col. 2, lines 18-21.

Therefore, it would have been obvious to enable gamma corrections in both the first and second processing circuits in Morris in addition to the existing circuits for further improving the first and second signals.

Regarding claim 6, see the analyses of claims 1 & 2.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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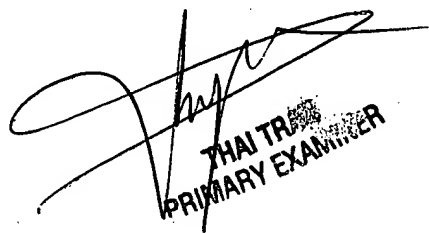
however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Thai Tran can be reached on (703) 305-4725. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.



THAI TRAN
PRIMARY EXAMINER